Development of a controlled High Voltage Power Supply for Gridded Ion Thrusters

IEPC-2017-337

Presented at the 35th International Electric Propulsion Conference
Georgia Institute of Technology – Atlanta, Georgia – USA
October 8–12, 2017

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Abstract: Operating a radio frequency ion thruster (RIT) requires a high voltage to extract ions out of the plasma. Used as a satellite propulsion system the high voltage has to be generated by means of the satellite power bus voltage as part of a power processing unit (PPU). Regarding power dissipation and thermal management a high efficiency is a major aspect in the design process.

This paper provides a transformer based circuit concept that implements a switch-mode power supply to create an adjustable high voltage. By taking benefit of certain discharge processes a zero-voltage switching (ZVS) of the semiconductor switches can be achieved and thereby the efficiency increased. A FPGA-based algorithm ensures the operation with reduced switching losses whenever it is possible.

Nomenclature

- $C_{DS}$ = parasitic drain source capacitance
- $C_F/L_F$ = filter capacitor / filter inductor
- $I_B$ = bridge current
- $I_{Limit}$ = minimum current required to discharge parasitic capacitance
- $L_e$ = equivalent inductance
- $L_{LK}$ = leakage inductance of the transformer
- $N$ = transformer turns ratio
- $N_{1/2}$ = number of turns in the transformer’s primary / secondary winding
- $R_e$ = equivalent ohmic resistor
- $R_L$ = load resistor
- $t_{A/B1}$ = locking-time of bridge leg A or B after low-side turn-off
- $t_{A/B2}$ = locking-time of bridge leg A or B after high-side turn-off
- $T_{ZV}$ = interval where zero voltage switching is possible
- $v_{A/B}$ = voltage between half bridge A or B output and DC link ground
- $v_{DS}$ = voltage across drain and source of a MOSFET
- $v_{GS,A/B±}$ = drive signal of high-side (+) or low-side (-) Mosfet in bridge leg A or B
- $v_{sec}$ = voltage across transformers secondary winding

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I. Introduction

Since the invention of the radio-frequency ion thruster by Horst Loeb in the 1960s, the Justus Liebig University of Giessen is doing research in the fields of plasma physics, alternative propellants and thruster modeling for simulation purposes. A cooperation with the University of Applied Sciences at Giessen extended the research area to studies and development of peripheral equipment necessary to operate this kind of thruster. The focus here is on power supply and control electronics. To reduce the power dissipation, electrical efficiency enhancement is a key factor in the development process of these devices. This not only minimizes the component stresses due to lower temperatures but also facilitates the thermal management when implemented into a satellite thruster system. The gain in reliability through reduced component stresses is another aspect of interest when working on this topic.

In order to meet these demands digital FPGA-based algorithms are used for controlling the switching of the power semiconductors of the converters. In conjunction with fast switching MOSFETs (metal-oxide-semiconductor field-effect-transistors) the turn-on and turn-off moments with lowest achievable switching losses can be determined with high accuracy. Using these techniques a radio-frequency generator supplying a RIT-10 and RIT-4 has already been developed and tested\(^2\). As a further step to an entire power processing unit (PPU) for ion thrusters a high voltage power supply is needed to generate voltages for the extraction grids. The necessary voltage level and also the current provided by the grid supply need to rise when higher specific impulses and an increase in thrust are required\(^3,4\). In addition, the ability to adjust the grid voltages over a certain range is crucial to ensure an optimal focused ion beam for maximizing the thruster’s lifetime and a precise control of the generated thrust. To satisfy these requirements, a digital controlled push-pull converter topology has been chosen as a basis for the development. Fundamental principles of operation were demonstrated using a first prototype. Especially, the control algorithm to ensure minimal switching losses is a major part within this paper.

The following sections describe the basic operation of the circuit topology including the low-loss switching technique and its implementation.

II. Theory of Operation

Considering the magnitude of the output voltage as a central design aspect of the converter and taking into account the required output current, a high-frequency transformer is used for boosting the input voltage level and energy transmission towards the load. An advantage of this approach compared to voltage doubling or diode-capacitor cascades is the ability to provide high output currents with a smaller voltage ripple. For an input voltage of 20V - 30V DC, that is usually employed in certain satellite applications\(^3\), an alternating voltage pattern has to be formed for operating the transformer. Using a full bridge circuit offers the possibility to create such an alternating pattern. Operating the transformer with that bipolar waveform the magnetic flux density inside the transformers core can change within the positive and negative saturation limits, increasing the maximum power transmitted. Rectification of the bipolar voltage at the secondary winding is attained by four diodes in full bridge configuration.

Due to the high turns ratio, a center tapped secondary winding using just two diodes will increase the transformers dimensions and weight, provided that the same voltage gain is required. In contrast to the center tapped solution, the additional two diodes of the full bridge rectifier will create an additional power loss that, however, has been taken into account.

The complete circuit concept is shown in Fig. 1. It corresponds to the push-pull converter topology published by Sabaté et al.\(^5\). There the circuit was used both to reduce the input voltage as well as to supply a load with high currents. In doing so, the transformer’s turns number on primary side is much greater than that on secondary side. Assuming an ideal transformer the following equation clarifies this relation:

\[
N = \frac{N_2}{N_1} = \frac{U_2}{U_1} = \frac{I_1}{I_2}. \tag{1}
\]

When used for generating high voltages, the number of turns in the secondary \(N_2\) has to be greater than the primary number of turns \(N_1\) leading to a high turns ratio \(N\). This causes the major differences during the design process compared to Sabaté et al.\(^5\). Taking into account the leakage inductance of the primary winding \(L_{LK}\) as well as parasitic capacitances of the semiconductor switches it is possible to reduce the power dissipation during the switching moment\(^6\).
A. Phase Shift Control

To illustrate the converter’s basic operation Fig. 2 shows some essential waveforms including bridge voltage $u_{\text{bridge}}$, transformer current $i_{\text{bridge}}$, and the control signals $v_{\text{GS}}$ of the power MOSFETs. $v_A$ and $v_B$ refer to the output voltage of both half-bridges with respect to dc link ground. The time intervals labeled by $S_1$ to $S_4$ represent the main switch states of the MOSFETs. During $S_1$ the switches $T_{A+}$ and $T_{B-}$ are closed, hence the dc link voltage is applied to the transformer. As a result the current $i_{\text{bridge}}$ rises depending on the load $R_L$, the filter inductor $L_F$ and the leakage inductance $L_{LK}$ of the transformer’s primary winding. Energy is transfered from the dc link voltage $V_{\text{DC}}$ to the load within this period. By turning off $T_{B-}$ the bridge current driven by $L_{LK}$ and $L_F$ commutates and diode $D_{B+}$ becomes conductive. During this free wheeling state $S_2$ the load resistor $R_L$ mainly determines the negative slope of $i_{\text{bridge}}$ (unless the current through the secondary transformer winding drops to zero). In case of $S_3$ a similar behavior to $S_1$ can be observed with a reversed polarity of $u_{\text{bridge}}$ and $i_{\text{bridge}}$. This also applies to $S_2$ and $S_4$. Looking at the secondary circuit the bipolar voltage pulses of $u_{\text{bridge}}$ are amplified by the transformer turns ratio $N$. In contrast to Fig. 2 the magnitude of these pulses is smaller than $V_{\text{DC}}$ because a notable voltage drop across $L_{LK}$ is caused by $i_{\text{bridge}}$ leading to a reduced voltage at the secondary winding. After rectification the unipolar pulse pattern is smoothed by the output filter consisting of $L_F$ and $C_F$.

Variation of $V_{\text{out}}$ is possible by adjusting the duration of the energy transfer states $S_1$ and $S_3$. This is achieved by shifting $v_B$ with respect to $v_A$ as shown in Fig. 2. Right shift of $v_B$ increases and left shift decreases the output voltage $V_{\text{out}}$. This phase shift modulation (PSM) is used to implement a closed loop
B. Discharge process during locking-time

To prevent a short of each half bridge a locking-time has to be inserted to separate the switching instants of \( T_{A+}, T_{A-} \) and \( T_{B+}, T_{B-} \), respectively. In Fig. 2 these transition periods are declared as \( t_{L,A1} \) and \( t_{L,B1} \) for the locking-time between low-side switch turn-off and high-side switch turn-on. \( t_{L,A2} \) and \( t_{L,B2} \) define the locking-time between high-side switch turn-off and low-side switch turn-on. During these intervals \( T_{A+}, T_{A-}, T_{B+}, T_{B-} \), respectively, are turned off and the corresponding output capacitances come into effect.

In combination with the transformer’s leakage inductance a resonant circuit is formed. Subsequently an oscillation is initiated which allows switching events with reduced switching losses, if the following turn-on moment satisfies a certain timing. As an example Fig. 3a allows a closer inspection during the transition from \( S_2 \) to \( S_3 \). It shows the equivalent model of the full bridge by solely including the relevant circuit elements within this interval. For simplification the transformer and all secondary-sided components are represented by the equivalent substitutes \( L_e \) and \( R_e \). In addition the parasitic drain source capacitances of the MOSFETs \( C_{A+} \) and \( C_{A-} \) are considered. At the beginning of \( S_3 \), \( C_{A+} \) is discharged and \( C_{A-} \) is fully charged to the dc link voltage level \( V_{DC} \). Turning off \( T_{A+} \), the current \( i_{bridge} \) will discharge \( C_{A-} \) and charge \( C_{A+} \). Consequently the voltage across \( T_{A-} \) drops according to Fig. 3b. Assuming the amount of \( i_{bridge} \) is high enough the capacitance \( C_{A-} \) can be fully discharged. As soon as \( V_{DS,T_{A-}} \) has become zero, \( T_{A-} \) can be switched on without switching loss (called zero-voltage switching, ZVS). The period of time while \( V_{DS,T_{A-}} \) is zero is named \( T_{ZV} \). However, the current \( i_{bridge} \) is required to meet a limit in order to enable ZVS. By means of energy analysis the required current can be estimated by the following equation

\[
I_{Limit} = \sqrt{\frac{2C_{DS}L_e}{V_{DC}}} \cdot V_{DC}. \tag{2}
\]

It assumes that \( C_{A-} \) is equal to \( C_{A+} \) and referred to as \( C_{DS} \). From Fig. 2, it can be seen that the available current at the switching moment of \( T_{A+} \) is determined by multiple factors. The slope of \( i_{bridge} \) during \( S_1 \) rises as the load current increases and specifies the maximum current at the end of \( S_1 \). Furthermore, the current slope within \( S_2 \) decreases with rising load current and leads to a higher \( i_{bridge} \) when entering \( S_3 \). As a result the energy stored in \( L_e \) is not sufficient for fully discharging the parasitic capacitance \( C_{A-} \) in case of light loads or small phase shift values. This case is also shown in Fig. 3b.

During turning on of half bridge B the current \( i_{bridge} \) is always at its maximum. For this reason, achieving ZVS is only critical for \( T_{A+} \) and \( T_{A-} \).
III. Implementation

To ensure, whenever possible, a zero voltage turn-on of $T_{A+}$ and $T_{A-}$ a closed loop control algorithm is used for adapting the locking-times $t_{L,A1}$ and $t_{L,A2}$. In this way, load changes and phase-shift variations can be compensated in terms of zero voltage switching. Fig. 4 illustrates the block diagram of the algorithm.

The primary measure used by the control loop is the voltage across $T_{A-}$. The voltages $v_{DS,TA+}, v_{DS,TA-}$ across $T_{A+}$ and $T_{A-}$, respectively, are measured, digitalized, and fed to the control algorithm. Accordingly, the digital signal $v_{A-}$ indicates whether the voltage across $T_{A-}$ is greater than or equal to zero. On the other hand $v_{A+}$ reflects whether the voltage across $T_{A+}$ is greater than or equal to zero.

### A. Zero-voltage Detection

To determine the time interval $T_{ZV}$ where the voltage across a switch is zero a zero-voltage detection unit is implemented. For clarification of its function, state $S_3$ according to Fig. 2 is inspected more closely. The first event, when entering this state, is turning off $T_{A+}$. This event is initiated by the falling edge of the digital control signal $v_{GS,A+}$ inside the FPGA. As shown in Fig. 4 the control signal $v_{GS,A+}$ is generated by the PWM generation unit for half bridge A and connected to the zero-voltage detection unit responsible for $T_{A-}$. In other words, the entrance into $S_3$ is indicated by the falling edge of $v_{GS,A+}$ but the subsequent turn on of $T_{A-}$ is desired. Consequently the zero-voltage detection unit for $T_{A-}$ is triggered by the falling edge of the complementary control signal $v_{GS,A-}$ and then observes the digital representation of the voltage across $T_{A-}$, named $v_{A-}$. If the voltage across $T_{A-}$ (referred to as $v_{DS,TA-}$) falls to zero, $v_{A-}$ changes to a logical high value and a counter inside the zero-voltage detection unit will be started. This counter is stopped by means of a logical low value of $v_{A-}$ (indicating a positive voltage across $T_{A-}$) or the rising edge of $T_{A-}$. The generated counter value $T_{ZV,A-}$ indicates the duration of a zero voltage across $T_{A-}$ after $T_{A+}$ turned off, further declared as zero voltage period. It corresponds to the number of clock cycles referring to the FPGAs system clock.

A similar detection unit is implemented for $T_{A+}$ and also shown in Fig. 4.

### B. ZVS Controller

Using the detected zero voltage period $T_{ZV,A-}$ the ZVS controller adapts the respective locking time, in this case $t_{L,A2}$. Handled by the PWM generation unit, the locking times $t_{L,A2}$ and $t_{L,A1}$ are converted into the corresponding temporal control signals $v_{GS,A+}$ and $v_{GS,A-}$. Fig. 5 illustrates the behavior of the ZVS controller for $T_{A-}$.

Assuming a small load current ZVS is not possible, referred to as case 1 in Fig. 5. Hence, there is no detected zero voltage period $T_{ZV,A-}$ because the counter inside the detection logic never starts. As a consequence the ZVS controller increases $t_{L,A2}$, assuming the positive edge of $v_{GS,A-}$ occurs too soon. When

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Figure 4: Block diagram of the ZVS control system

The 35th International Electric Propulsion Conference, Georgia Institute of Technology, USA
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reaching a predefined limit $t_{L,A2,\text{max}}$, the incrementation of $t_{L,A2}$ stops. A rising load current allowing ZVS will affect the waveform of $v_{DS,TA-}$ as shown in case 2. A positive zero voltage period $T_{ZV,A-}$ will be detected but the rising edge of $v_{GS,A-}$ is outside that range. Therefore the ZVS Controller gradually decreases the locking time $t_{L,A2}$ until a zero voltage period $T_{ZV,A-}$ of one count is detected, that corresponds to case 3. Now the rising edge of $v_{GS,A-}$ is located within the zero voltage period and ZVS is realized for $T_{A-}$. A falling load current below the ZVS limit leads to case 4. The previous value of $t_{L,A2}$ will be increased again until $t_{L,A2,\text{max}}$ is reached.

Furthermore, the ZVS controller ensures a minimal locking time $t_{L,A2,\text{min}}$ to prevent cross currents through the half bridge. The same applies to the ZVS controller of $T_{A+}$.

When zero-voltage switching is found to be possible for the current point of operation, the algorithm will establish ZVS after a few switching cycles of the converter. The achievable temporal resolution depends on the FPGAs system clock. In the current application a frequency of 200 MHz is used to operate the control logic so the locking-times can be adapted in steps of 5 ns.

### IV. Hardware Assembly and Measurement

#### A. ZVS Control Algorithm

To verify the proper functioning of the ZVS control algorithm, the high voltage generator as shown in Fig. 1 is operated with a fixed phase-shift of $PS = 0.1$ referred to the switching period (36 degree) while the load current rises.

Initially a load resistance of $R_L = 2.2 \, \text{kΩ}$ is applied. Fig. 6a shows both the voltage across $T_{A+}$ ($v_{DS,TA-}$) and the control signals $v_{GS,A+}$ and $v_{GS,A-}$ for that point of operation. The locking-time $t_{L,A2}$ reaches the maximum limit of 320 ns determined by the control logic because $v_{DS,TA-}$ never falls to zero during that period and ZVS is not possible. Furthermore, the dead time between the control signal edge and the switching moment of the MOSFET can be measured to approx. 35 ns. Immediately after reducing the load resistor to 1.3 kΩ, $v_{DS,TA-}$ falls to zero as shown in Fig. 6b. Thus, the zero-voltage detection logic recognizes a positive value of $T_{ZV,A-}$ and the ZVS controller decrements the locking-time $t_{L,A2}$ every switching cycle. If a zero-voltage time $T_{ZV,A-}$ of 5 ns (respectively one FPGA clock cycle) is reached, the ZVS Controller will stop reducing the locking-time. Fig. 6c shows the steady state with a $t_{L,A2}$ of 155 ns. The further reduction of $R_L$ down to 1.0 kΩ is shown in Fig. 6d. However the zero-voltage time $T_{ZV,A-}$ is not equal to the desired 5 ns but approx. 30 ns. This might be caused by the dead-time of the digitizer converting $v_{DS,TA-}$ to the digital representation $v_{A-}$. Nonetheless $t_{L,A2}$ is adapted depending on the load confirming the functioning of the ZVS control algorithm and of the basic hardware assembly.
(a) Light load operation ($R_L = 2.2 \, k\Omega$)

(b) Immediately after load step ($R_L = 1.3 \, k\Omega$)

(c) Steady state of ZVS Controller after load step ($R_L = 1.3 \, k\Omega$)

(d) Steady state of ZVS Controller with $R_L = 1.0 \, k\Omega$

Figure 6: Measured waveforms of $v_{DS,TA}$ (deep blue), $v_{GS,A-}$ (green) and $v_{GS,A+}$ (light blue)

B. Hardware Assembly

The prototype assembly is shown in Fig. 7. A modular design concept is used to split control and power circuits. The FPGA module is the centerpiece of the control circuit. It implements the digital control logic, further peripherals as well as certain interfaces used for reconfiguration, communication, and diagnostics. To interact with the power circuit an edge-mount connector provides the port signals of the FPGA. This kind of connector allows a pluggable attachment of the power board and offers the possibility to use the control circuit in conjunction with various power board configurations.

The power board used for the high voltage power supply implements a full bridge topology by utilizing GaN-based MOSFETs. Due to switching times down to several nanoseconds (see Fig. 6a) the power dissipation of a switching moment is reduced in comparison with conventional MOSFETS even if no ZVS is applied. Nevertheless a heat sink is mounted onto the power semiconductors to fulfill cooling purposes in high power applications. Regarding the gate drive circuit multiple galvanically isolated supplies are used for both high-side and the low-side switch. The control signals are transmitted by digital isolators between the different power domains. This causes a propagation delay of approx. 35 ns as shown in Fig. 6a but ensures reliable decoupling of the drive signals belonging to the same half bridge. Transformer, rectifier, and filter circuit are mounted on a screwable breadboard. Silicon carbide diodes used for rectification allow high switching frequencies beyond 100 kHz. Currently the high frequency transformer has a turns ratio of $N = 25$. Assuming the ideal transformer model, no load and neglecting parasitic effects a maximum output voltage of up to 500 V can be generated.

V. Conclusion and Outlook

In this paper a high voltage power supply concept has been presented. Focusing on reducing switching losses, an algorithm is implemented and its functioning verified. The theory behind this approach yields a better understanding of the control mechanism.

Nonetheless, there are various points for further investigation. In order to classify the advantages in
reduced power dissipation by applying the presented algorithm, further measurements regarding the efficiency have to be carried out. Furthermore, supplying an ion thruster requires voltages up to 2000 V. To achieve this, the turns ratio \( N \) of the transformer needs to be increased. Replacing the present transformer by an alternative part is one task for further work. An additional feature of the FPGA-based logic is the variation of the switching frequency. This offers the possibility to implement advanced concepts for a further reduction of switching losses.

References